



Akihiro Hayashi, Ph.D.

Research Scientist, Rice University

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Summary

Dr. Hayashi is a research scientist at Rice university. He has over eight years of experience in conducting and leading research in the Programming Languages and Parallel Computing areas. His research interests include automatic parallelization and programming languages and compiler optimizations for parallel computer systems.

Professional Experience

RESEARCH SCIENTIST, RICE UNIVERSITY, HOUSTON, TX, USA – 2015-PRESENT

Responsible for conducting and leading research on 1) LLVM-based optimizations for large-scale systems, 2) code generation and optimizations for Graphics Processing Units (GPUs), and 3) automatic construction of compiler/runtime heuristics using machine-learning techniques.

CAS RESEARCH FELLOW, IBM CENTERS FOR ADVANCED STUDIES, TORONTO, CANADA – 2014-PRESENT

Responsible for leading an IBM CAS research fellowship project titled “GPU Enablement of Java Applications”, which aims to add a capability of generating GPU code to IBM’s Java compiler and virtual machine. I personally work on 1) compiling and optimizing Java 8 programs for GPU execution, and 2) constructing performance heuristics that select a preferable computing resource using machine-learning techniques.

POSTDOCTORAL RESEARCHER, RICE UNIVERSITY, HOUSTON, TX USA – 2013-2015

Conducted research in the area of compiler and runtime support for parallel languages such as Habanero-Java. In particular, I worked on high-level language constructs and parallel code generation for GPUs while maintaining precise exception semantics on GPUs.

ASSISTANT PROFESSOR, WASEDA UNIVERSITY, TOKYO, JAPAN – 2012-2013

Conducted research on automatic parallelizing compiler and compiler-directed power reduction techniques in collaboration with many companies in Japan. More specifically, I worked on parallelizing and optimizing 1) automotive engine control softwares with TOYOTA and Denso, 2) a dose calculation software for heavy-ion therapy with Mitsubishi Electric, 3) smartphone applications on Android platform with Fujitsu Ltd., and 4) multimedia applications with Olympus Corporation.

Instructor for freshman-level 1) computer literacy class and 2) programming class with C language in Spring/Fall 2012.



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RESEARCH ASSOCIATE, WASEDA UNIVERSITY, TOKYO, JAPAN – 2010-2012

Conducted research on automatic parallelization and power reduction techniques for embedded heterogeneous multi-core processors. In addition, I worked on the automatic parallelization and optimization of a clinically-used dose calculation software for heavy-ion therapy in collaboration with Mitsubishi Electric. Based on experimental results on an IBM POWER7 platform, our optimized version was over 50x faster than the conventional version.

RESEARCH ASSOCIATE , GLOBAL COE PROGRAM, WASEDA UNIVERSITY, TOKYO, JAPAN – 2007-2010

Conducted research on automatic parallelization and power reduction techniques for embedded heterogeneous multi-core processors in collaboration with Hitachi Ltd. and Renesas Electronics Corporation (formerly known as Renesas Technology). This work was partially supported by one of the global centers of excellence (GCOE) program named "International research and education center for Ambient SoC" established by Japan's Ministry of Education, Culture, Sports, Science and Technology (MEXT).

Education

PH.D., COMPUTER SCIENCE, WASEDA UNIVERSITY, TOKYO, JAPAN – 2012

Thesis : "Studies on Automatic Parallelization for Heterogeneous and Homogeneous Multicore Processors"

Advisor : Professor Hironori Kasahara

M.E., COMPUTER SCIENCE, WASEDA UNIVERSITY, TOKYO, JAPAN – 2008

Thesis : "Study on Compiler Cooperative Heterogeneous Multicore Architecture"

Advisor : Professor Hironori Kasahara

B.E., COMPUTER SCIENCE, WASEDA UNIVERSITY, TOKYO, JAPAN – 2007

Thesis : "Parallel Code Generation Scheme for Hierarchical Multigrain Parallel Processing on Heterogeneous Multicore Processor"

Advisor : Professor Hironori Kasahara



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Awards

- ▶ Encouragement award, IPSJ Symposium on Embedded Systems, October 2013.
(Dan Umeda, Yohei Kanehagi, Hiroki Mikami, Akihiro Hayashi, Mitsuhiro Tani, Hiroshi Mori, Keiji Kimura, Hironori Kasahara)
- ▶ Best feature award, COOL Chips XVI, IEEE Symposium on Low Power and High-Speed Chips, April 2013.
(Yohei Kishimoto, Hiroki Mikami, Keiichi Nakano, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara,)
- ▶ Encouragement award, IPSJ Symposium on Embedded Systems, October 2012.
(Yohei Kishimoto, Hiroki Mikami, Keiichi Nakano, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara)
- ▶ IPSJ SIG recommended Ph.D thesis, September 2012.
- ▶ Best presentation award, 5th GCOE Symposium, September 2009.

Industry Gifts

- ▶ IBM CAS Fellowship for research on "Automatic Runtime Parallelization of JVM Applications" by Max Grossman, (PI: Vivek Sarkar, Co-PI: Akihiro Hayashi), 2016, \$20,000.
- ▶ IBM CAS Fellowship for research on "GPU Enablement of Java Applications" by Akihiro Hayashi, 2015, \$28,000.
- ▶ IBM CAS Fellowship for research on "GPU Enablement of Java Applications" by Akihiro Hayashi, 2014, \$28,000.

Program Committees

- ▶ Program Committee Member, 22nd ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP), March 2017.
- ▶ Program Committee Member, 22nd IEEE International Conference on Parallel and Distributed Systems (ICPADS), December 2016.



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- ▶ Program Committee Member, 3rd International Workshop on Software Engineering for Parallel Systems (SEPS), November 2016 (co-located with SPLASH2016).
- ▶ Technical Program Committee Member, 29th IEEE International Parallel & Distributed Processing Symposium (IPDPS), May 2015.
- ▶ Program Committee Member, IPSJ Symposium on Advanced Computing Systems and Infrastructures (SACSYS), May 2013.
- ▶ Local arrangement Co-chair, 25th International Workshop on Languages and Compilers for Parallel Computing (LCPC), September 2012.

External Reviewers

- ▶ International Conference on Network and Parallel Computing (NPC2016)
- ▶ International Conference on Parallel Processing (ICPP2016)
- ▶ International Conference on Parallel Architectures and Compilation Techniques (PACT2015)
- ▶ International Conference for High Performance Computing, Networking, Storage and Analysis (SC13)
- ▶ International Conference on Supercomputing (ICS2013)
- ▶ International Conference on Parallel and Distributed Systems (ICPADS2013)
- ▶ International Conference on Computer Design (ICCD2014, ICCD2013, ICCD2012)
- ▶ International Workshop on Languages and Compilers for Parallel Computing (LCPC2015, LCPC2014, LCPC2013)
- ▶ IPSJ (Information Processing Society of Japan) Journals (2014)
- ▶ IEICE (The Institute of Electronics, Information and Communication Engineers) Transactions on Information and Systems (2013, 2012)



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Courses

- ▶ Computer Literacy, Waseda University, Spring 2012. (English Course)
- ▶ C Programming, Waseda University, Fall 2012. (English Course)
- ▶ Science and Engineering Lab., Waseda University, Spring/Fall 2012. (Japanese Course)

Other Remarkable Experience

- ▶ Co-founder of interdisciplinary research group named WIZDOM, inspired by FabLab at MIT, officially supported by department of computer science, Waseda University.

Skills

- ▶ Programming Languages (C/C++, Java, Python)
- ▶ Parallel Programming Languages (X10, Chapel, UPC/UPC++, Habanero-Java)
- ▶ Compilers (LLVM, Soot)



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Refereed Conference and Journal Publications

1. **Compiling and Optimizing Java 8 Programs for GPU execution.** Kazuaki Ishizaki, Akihiro Hayashi, Gita Koblents, Vivek Sarkar. 24th International Conference on Parallel Architectures and Compilation Techniques (PACT2015), October 2015.
2. **Machine-Learning-based Performance Heuristics for Runtime CPU/GPU Selection.** Akihiro Hayashi, Kazuaki Ishizaki, Gita Koblents, Vivek Sarkar. 12th International Conference on the Principles and Practice of Programming in Java (PPPJ2015), September 2015.
3. **Automatic Parallelization of Designed Engine Control C Codes by MATLAB/Simulink.** Dan Umeda, Yohei Kanehagi, Hiroki Mikami, Akihiro Hayashi, Mitsuhiro Tani, Hiroshi Mori, Keiji Kimura, Kasahara Hironori, IPSJ Journal, August, 2014. (in Japanese)
4. **Accelerating Habanero-Java Program with OpenCL Generation.** Akihiro Hayashi, Max Grossman, Jisheng Zhao, Jun Shirako, Vivek Sarkar. 10th International Conference on the Principles and Practice of Programming in Java (PPPJ2013), September 2013.
5. **Automatic Parallelization, Performance Predictability and Power Control for Mobile-Applications.** Dominic Hillenbrand, Akihiro Hayashi, Hideo Yamamoto, Keiji Kimura, Hironori Kasahara. 16th IEEE Symposium on Low-Power and High-Speed Chips (CoolChips XVI), April 2013.
6. **Parallelization of Automotive Engine Control Software On Embedded Multi-core Processor Using OSCAR Compiler.** Yohei Kanehagi, Dan Umeda, Akihiro Hayashi, Keiji Kimura and Hironori Kasahara, 16th IEEE Symposium on Low-Power and High-Speed Chips (CoolChips XVI), April 2013.
7. **Parallel processing of multimedia applications on TILEPro64 using OSCAR API for embedded multicore.** Yohei Kishimoto, Hiroki Mikami, Keiichi Nakano, Akihiro Hayashi, Keiji Kimura and Hironori Kasahara, IPSJ Symposium on Embedded System (ESS2012), October 2012. (in Japanese)
8. **Automatic Parallelization of Dose Calculation Engine for A Particle Therapy.** Akihiro Hayashi, Takuji Matsumoto, Hiroki Mikami, Keiji Kimura, Keiji Yamamoto, Hironori Saki, Yasuyuki Takatani, Hironori Kasahara, IPSJ Symposium on High Performance Computing and Computer Science (HPCS2012), January 2012. (in Japanese)

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9. **Parallelizing Compiler Framework and API for Heterogeneous Multicores.** Akihiro Hayashi, Yasutaka Wada, Takeshi Watanabe, Takeshi Sekiguchi, Masayoshi Mase, Jun Shirako, Keiji Kimura and Hironori Kasahara, IPSJ Transactions on Advanced Computing Systems (ACS), Vol.5, No.1, pp.68-79, November 2011. (in Japanese)
10. **A Parallelizing Compiler Cooperative Heterogeneous Multicore Processor Architecture.** Yasutaka Wada, Akihiro Hayashi, Takeshi Masuura, Jun Shirako, Hirofumi Nakano, Hiroaki Shikano, Keiji Kimura, and Hironori Kasahara, Transactions on High-Performance Embedded Architectures and Compilers IV (HiPEAC IV), Lecture Note in Computer Science, Springer, Vol. 6760, pp. 215-233, November 2011.
11. **A 45nm Heterogeneous Multi-core SoC Supporting an over 32-bits Physical Address Space for Digital Appliance.** Takumi Nito, Yoichi Yuyama, Masayuki Ito, Yoshikazu Kiyoshige, Yusuke Nitta, Osamu Nishii, Atsushi Hasegawa, Makoto Ishikawa, Tetsuya Yamada, Junichi Miyakoshi, Koichi Terada, Tohru Nojiri, Masashi Takada, Makoto Satoh, Hiroyuki Mizuno, Kunio Uchiyama, Yasutaka Wada, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara, Hideo Maejima, 13th IEEE Symposium on Low-power and High-Speed Chips (COOL Chips XIII), April 2010.
12. **Parallelization of MP3 Encoder using Static Scheduling on a Heterogeneous Multicore.** Yasutaka Wada, Akihiro Hayashi, Takeshi Masuura, Jun Shirako, Hirofumi Nakano, Hiroaki Shikano, Keiji Kimura, Hironori Kasahara, Transactions of IPSJ on Computing Systems, Vol. 49 (ACS), 2008 (in Japanese)
13. **Software-Cooperative Power-Efficient Heterogeneous Multi-Core for Media Processing.** Hiroaki Shikano, Masaki Ito, Kunio Uchiyama, Toshihiko Odaka, Akihiro Hayashi, Takeshi Masuura, Masayoshi Mase, Jun Shirako, Yasutaka Wada, Keiji Kimura, Hironori Kasahara, 13th Asia and South Pacific Design Automation Conference (ASP-DAC2008), January 2008.



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Refereed Workshop Proceedings

1. **Exploring Compiler Optimization Opportunities for the OpenMP 4.x Accelerator Model on a POWER8+GPU Platform.** Akihiro Hayashi, Jun Shirako, Ettore Tiotto, Robert Ho, Vivek Sarkar. 3rd Workshop on Accelerator Programming Using Directives (WACCPD), November 2016. (co-located with SC16)
2. **LLVM-based Communication Optimizations for PGAS Programs.** Akihiro Hayashi, Jisheng Zhao, Michael Ferguson, Vivek Sarkar. 2nd Workshop on the LLVM Compiler Infrastructure in HPC (LLVM), November, 2015. (co-located with SC15)
3. **LLVM Optimizations for PGAS Programs -Case Study: LLVM Wide Optimization in Chapel-.** Akihiro Hayashi, Rishi Surendran, Jisheng Zhao, Michael Ferguson, Vivek Sarkar. 1st Chapel Implementers and Users Workshop (CHI UW2014), May 2014. (co-located with IPDPS)
4. **Speculative Execution of Parallel Programs with Precise Exception Semantics on GPUs.** Akihiro Hayashi, Max Grossman, Jisheng Zhao, Jun Shirako, Vivek Sarkar. 26th International Workshop on Languages and Compilers for Parallel Computing (LCPC2013), September 2013. (co-located with CnC).
5. **Reconciling Application Power Control and Operating Systems for Optimal Power and Performance.** Dominic Hillenbrand, Yuuki Furuyama, Akihiro Hayashi, Mikami Hiroki, Keiji Kimura, Hironori Kasahara. 8th International Workshop on Reconfigurable Communication-centric Systemson-Chip (ReCoSoC2013), Germany, 2013.
6. **Automatic Parallelization of Hand Written Automotive Engine Control Codes Using OSCAR Compiler.** Dan Umeda, Yohei Kanehagi, Hiroki Mikami, Akihiro Hayashi, Keiji Kimura and Hironori Kasahara. 17th Workshop on Compilers for Parallel Computing (CPC2013), July 2013.
7. **OSCAR API v2.1: Extensions for an Advanced Accelerator Control Scheme to a Low-Power Multicore API.** Keiji Kimura, Cecilia Gonzales-Alvarez, Akihiro Hayashi, Hiroki Mikami, Mamoru Shimaoka, Jun Shirako, Hironori Kasahara, 17th Workshop on Compilers for Parallel Computing (CPC2013), July 2013.
8. **Automatic Design Exploration Framework for Multicores with Reconfigurable Accelerators.** Cecilia Gonzalez-Alvarez, Haruku Ishikawa, Akihiro Hayashi, Daniel

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- Jimenez-Gonzalez, Carlos Alvarez, Keiji Kimura and Hironori Kasahara. 7th HiPEAC Workshop on Reconfigurable Computing (WRC2013), January, 2013.
9. **OSCAR Parallelizing Compiler and API for Real-time Low Power Heterogeneous Multicores.** Akihiro Hayashi, Mamoru Shimaoka, Hiroki Mikmi, Masayoshi Mase, Yasutaka Wada, Jun Shirako, Keiji Kimura, and Hironori Kasahara, 16th Workshop on Compilers for Parallel Computing (CPC2012), January 2012.
 10. **Evaluation of Power Consumption at Execution of Multiple Automatically Parallelized and Power Controlled Media Applications on the RP2 Low-power Multicore.** Hiroki Mikami, Shumpei Kitaki, Masayoshi Mase, Akihiro Hayashi, Mamoru Shimaoka, Keiji Kimura, Masato Edahiro, and Hironori Kasahara, 24th International Workshop on Languages and Compilers for Parallel Computing (LCPC2011), September 2011.
 11. **Parallelizing Compiler Framework and API for Power Reduction and Software Productivity of Real-time Heterogeneous Multicores.** Akihiro Hayashi, Yasutaka Wada, Takeshi Watanabe, Takeshi Sekiguchi, Masayoshi Mase, Jun Shirako, Keiji Kimura and Hironori Kasahara, 23rd International Workshop on Languages and Compilers for Parallel Computing (LCPC2010), October 2010.
 12. **Performance of OSCAR Multigrain Parallelizing Compiler on Multicore Processors.** Hiroki Mikami, Jun Shirako, Masayoshi Mase, Takamichi Miyamoto, Hirofumi Nakano, Fumiyo Takano, Akihiro Hayashi, Yasutaka Wada, Keiji Kimura, Hironori Kasahara, 14th Workshop on Compilers for Parallel Computing(CPC2009), January 2009.
 13. **Parallelizing Compiler Cooperative Heterogeneous Multicore.** Yasutaka Wada, Akihiro Hayashi, Takeshi Masuura, Jun Shirako, Hirofumi Nakano, Hiroaki Shikano, Keiji Kimura, Hironori Kasahara, Workshop on Software and Hardware Challenges of Manycore Platforms (SHCMP2008), June 2008. (co-located ISCA2008)



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Refereed Posters

1. **How Java runtime can execute practical Java programs on GPU.** Kazuaki Ishizaki, Gita Koblents, Akihiro Hayashi, Vivek Sarkar, Hiroshi Inoue. Poster Session, IPSJ Symposium on High Performance Computing and Computer Science (HPCS2015), May 2015. (in Japanese)
2. **Parallel Processing of Multimedia Applications on TILEPro64.** Yohei Kishimoto, Hiroki Mikami, Keiichi Nakano, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara. 16th IEEE Symposium on Low Power and High-Speed Chips (COOL Chips XVI), April 2013.
3. **Opportunities and Challenges of Application-Power Control in the Age of Dark Silicon.** Dominic Hillenbrand, Yuuki Furuyama, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara. 8th international conference on High-Performance and Embedded Architectures and Compilers (HiPEAC2013), January 2013.
4. **OSCAR Parallelizing Compiler Cooperative Heterogeneous Multi-core Architecture.** Akihiro Hayashi, Yasutaka Wada, Hiroaki Shikano, Teruo Kamiyama, Takeshi Watanabe, Takeshi Sekiguchi, Masayoshi Mase, 18th International Conference on Parallel Architectures and Compilation Techniques (PACT2009), September 2009.

Invited Talks

1. **How to design human actions by digital technology?** The National Convention of IPSJ, March 2013. (in Japanese)

Presentations

1. **Machine-learning-based Performance Heuristics for Runtime CPU/GPU Selection in Java.** 10th Workshop on Challenges for Parallel Computing, November 2015. (co-located with IBM CASCON2015)
2. **LLVM-based Communication Optimizations for Chapel.** Chapel Lightning Talks Birds-of-a-Feather at International Conference for High Performance Computing, Networking, Storage and Analysis (SC14), November 2014.



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Non Refereed Technical Reports

1. **Performance Evaluation of Hierarchical Barrier Hardware with OSCAR API Analyzer.** Akihiro Kawashima, Yohei Kanehagi, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ. Vol.2013-ARC-206-16 (SWoPP2013), July 2013. (in Japanese)
2. **An Investigation of Parallelization and Evaluation on Commercial Multi-core Smart Device.** Hideo Yamamoto, Takashi Goto, Tomohiro Hirano, Kouhei Muto, Hiroki Mikami, Dominic Hillenbrand, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol. 2013-OS-124, February 2013. (in Japanese)
3. **Parallelization of Automobile Engine Control Software on Multicore Processor.** Yohei Kanehagi, Dan Umeda, Hiroki Mikami, Akihiro Hayashi, Mitsuo Sawada, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2013-ARC195-2, January 2013. (in Japanese)
4. **Automatic parallelization of the GMS Earthquake simulator with OSCAR Compiler.** Mamoru Shimaoka, Hiroki Mikami, Akihiro Hayashi, Yasutaka Wada, Keiji Kimura, Hidekazu Morita, Kunio Uchiyama, Hironori Kasahara. Technical Report of IPSJ, Vol. 2012-ARC194HPC137-26 (HOKKE2012), December 2012.
5. **Automatic parallelization with OSCAR API Analyzer: a cross-platform performance evaluation.** Cecilia Gonzalez-Alvarez, Yohei Kanehagi, Kosei Takemoto, Yohei Kishimoto, Kohei Muto, Hiroki Mikami, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2012-ARC194HPC137-10 (HOKKE2012), December 2012.
6. **Opportunities and Challenges of Application-Power Control in the Age of Dark Silicon.** Dominic Hillenbrand, Yuuki Furuyama, Akihiro Hayashi, Hiroki Mikami, Keiji Kimura, Hironori Kasahara, Technical Report of IPSJ, Vol.2012-ARC194HPC137-11(HOKKE2012), December 2012.
7. **Realization of 1 Watt Web Service with RP-X Low-power Multicore Processor.** Yuuki Furuyama, Mamoru Shimaoka, Hiroki Mikami, Akihiro Hayashi, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2012-ARC-201-24 (SWoPP2012), August 2012. (in Japanese)

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8. **Parallelization of Basic Engine Control Software Model on Multicore Processor.** Dan Umeda, Yohei Kanehagi, Hiroki Mikami, Akihiro Hayashi, Mituhiro Tani, Yuji Mori, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2012-ARC-201-22 (SWoPP2012), August 2012. (in Japanese)
9. **Automatic Parallelization of Dose Calculation Engine for A Particle Therapy on SMP Servers.** Akihiro Hayashi, Takuji Matsumoto, Hiroki Mikami, Keiji Kimura, Keiji Yamamoto, Hironori Saki, Yasuyuki Takatani, Hironori Kasahara. Technical Report of IPSJ, Vol.2011-ARC189HPC132-2 (HOKKE2011), November 2011. (in Japanese)
10. **Hiding I/O overheads with Parallelizing Compiler for Media Applications.** Akihiro Hayashi, Takeshi Sekiguchi, Masayoshi Mase, Yasutaka Wada, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2011-ARC-195OS117-14, April 2011. (in Japanese)
11. **Evaluation of Parallelizable C Programs by the OSCAR API Standard Translator.** Takuya Sato, Hiroki Mikami, Akihiro Hayashi, Masayoshi Mase, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2010-ARC-191-2, October 2010. (in Japanese)
12. **A Compiler Framework for Heterogeneous Multicores for Consumer Electronics.** Akihiro Hayashi, Yasutaka Wada, Takeshi Watanabe, Takeshi Sekiguchi, Masayoshi Mase, Keiji Kimura, Masayuki Ito, Jun Hasegawa, Makoto Sato, Toru Nojiri, Kunio Uchiyama, Hironori Kasahara. Technical Report of IPSJ, Vol.2010-ARC-190-7 (SWoPP2010), August 2010. (in Japanese)
13. **Performance of Power Reduction Scheme by a Compiler on Heterogeneous Multicore for Consumer Electronics RP-X.** Yasutaka Wada, Akihiro Hayashi, Takeshi Watanabe, Takeshi Sekiguchi, Masayoshi Mase, Jun Shirako, Keiji Kimura, Masayuki Ito, Jun Hasegawa, Makoto Sato, Toru Nojiri, Kunio Uchiyama, Hironori Kasahara, Technical Report of IPSJ, Vol.2010-ARC-190-8 (SWoPP2010), August 2010. (in Japanese)
14. **Performance Evaluation of Parallelizing Compiler Cooperated Heterogeneous Multicore Architecture Using Media Applications.** Teruo Kamiyama, Yasutaka Wada, Akihiro Hayashi, Masayoshi Mase, Hirofumi Nakano, Takeshi Watanabe, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2009-ARC-173, Jan. 2009. (in Japanese)

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15. **A Hierarchical Coarse Grain Task Static Scheduling Scheme on a Heterogeneous Multicore.** Yasutaka Wada, Akihiro Hayashi, Taketo Iyoku, Jun Shirako, Hirofumi Nakano, Hiroaki Shikano, Keiji Kimura, Hironori Kasahara, Technical Report of IPSJ, Vol.2007-ARC-174-17 (SWoPP2007), August 2007. (in Japanese)
16. **Compiler Control Power Saving for Heterogeneous Multicore Processor.** Akihiro Hayashi, Taketo Iyoku, Ryo Nakagawa, Shigeru Matsumoto, Kaito Yamada, Naoto Oshiyama, Jun Shirako, Yasutaka Wada, Hirofumi Nakano, Hiroaki Shikano, Keiji Kimura, Hironori Kasahara. Technical Report of IPSJ, Vol.2007-ARC-174-18 (SWoPP2007), August 2007. (in Japanese)



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Software Artifacts

- ▶ Contributed to IBM Java compiler/VM (IBM).
- ▶ Contributed to Cray Chapel compiler (Cray Inc.).
- ▶ Contributed to Habanero-Java compiler/runtime (Rice University).
- ▶ Contributed to OSCAR parallelizing compiler (Waseda University).